

A Vertical SiC JFET with a Monolithically Integrated JBS Diode

K. Sheng, R. Radhakrishnan, Y. Zhang and J.H. Zhao
Electr. & Comp. Eng. Dept, Rutgers University, Piscataway, NJ, 08854, USA
email: ksheng@ece.rutgers.edu

Abstract—It is desirable for many power applications to integrate a power switch and its reverse-parallel diode onto the same chip/package to reduce component count and improve circuit reliability and integrity. In this paper, a SiC vertical JFET with a monolithically integrated JBS diode is proposed, fabricated and characterized. The integrated switch uses a process similar to that of a traditional SiC vertical JFET. The experimental results show that, in the reverse direction, the integrated switch, can conduct current by utilizing both the integrated diode and the JFET channel. This can be utilized to significantly reduce the device conduction loss in power electronic applications.

I. INTRODUCTION

In most power electronic applications, a diode is usually required to be anti-parallel connected to a power switch to provide a possible free-wheeling path of the load current. Such a diode usually needs to possess properties such as low conduction loss, high blocking voltage and fast reverse recovery, which requires separate optimization of the diode structural parameters. Since the body diode of a power MOSFET does not normally provide these qualifications, a separate diode is also needed. A lot of manufacturers combine the power switch and its anti-parallel diode in the same package.

To reduce component count, reduce circuit parasitics, improve reliability and reduce cost, it is desirable to have a device with an integrated reverse diode that is able to give the above-mentioned qualifications. SiC Schottky Barrier Diode (SBD) is an attractive diode as it is the only commercially-available high voltage unipolar diode, which means it has “virtually-zero” reverse recovery charge. Combination of a SiC unipolar power switch with a SiC SBD gives the ideal pair for power electronics.

A recent paper has reported a SiC BJT with an integrated SBD [1]. As the BJT and the SBD were not able to share many process steps, the fabrication process used for this device was significantly more involved than either BJT or SBD and the final device were not able to block voltage.

In this paper, it is proposed to monolithically integrated a SiC vertical JFET with a SiC SBD as the same device with a process that requires only one step more than a simple SiC

JFET. The fabrication steps will be explained in detail and the fabricated device will be characterized for its functionality.

II. DEVICE STRUCTURE AND FABRICATION

A. Device Structure

The cross-sectional view of the proposed integrated device and its circuit symbol is shown in Fig. 1. The structure of the power switch is based on that of a trench-and-implanted vertical JFET (TI-VJFET) previously reported in multiple papers [2,3]. It can be seen that the VJFET and the SBD shares a very similar structure with the only difference being that the source/anode metal makes ohmic contact to an N⁺ region in the VJFET while it makes a Schottky contact to an N region in the SBD. The same trench-and-implanted process used for the VJFET is utilized to make P⁺ regions for the Schottky Barrier Diode, effectively making it a Junction Barrier Schottky (JBS) diode. These deep JBS P⁺ regions provide a better potential barrier than simple implanted P⁺ regions of a normal JBS diode. The great similarity between the structures of the VJFET and the JBS achieves maximum sharing of processing steps between the two and minimizes additional processing complexity. This is a clear advantage over the BJT/SBD integration scheme. Another important advantage of this approach is that the JFET can be effectively used with the “synchronous rectification” circuit technique [4]. In this mode, the JFET gate is turned on when the anti-parallel diode is conducting current, helping to significantly reduce forward conduction voltage of the diode. This technique is frequently used in power electronic circuits such as some DC/DC converters and inverters.

B. Device Fabrication

The starting material has an 11 μm , $9 \times 10^{15} \text{cm}^{-3}$ N⁻ drift region epi, a 2.5 μm , $6 \times 10^{16} \text{cm}^{-3}$ channel N epi and a 0.7 μm $> 1 \times 10^{19} \text{cm}^{-3}$ N⁺ top ohmic contact epi. The main processing steps involved include trench etching, P⁺ implantation, implantation annealing, mesa top removal, JBS N⁺ removal, oxidation, surface passivation, JFET window opening, ohmic contact metal deposition, backside and front-side ohmic contact annealing, trench filling, planarization, via window opening and final metal overlay.

These processing steps are almost identical to those of a single TI-VJFET [2,3] with only one additional step of

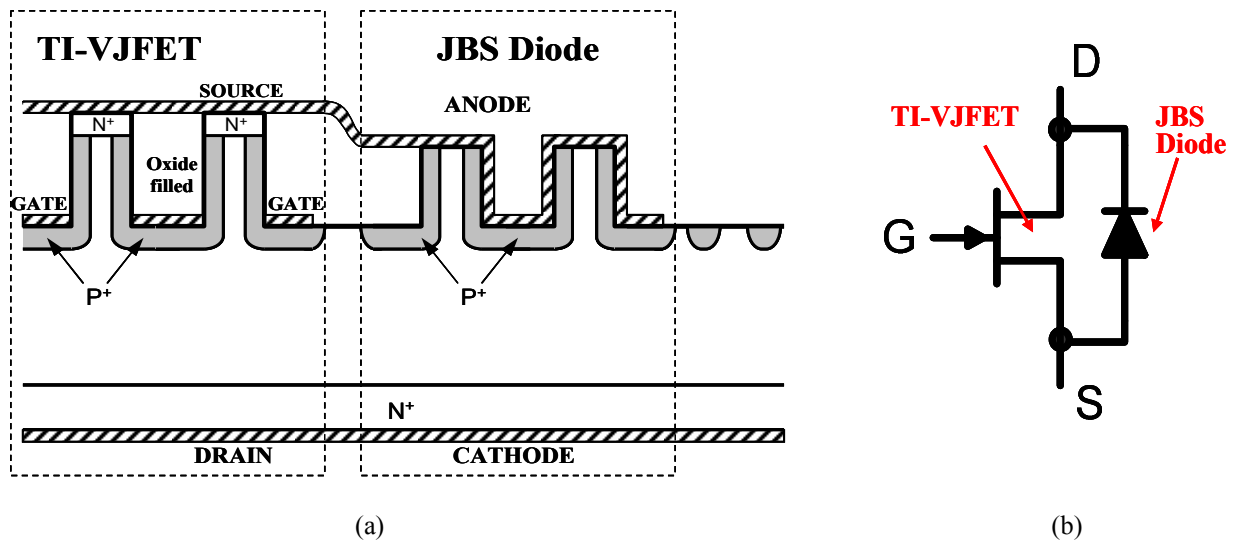


Fig. 1 (a), Cross-sectional view of the integrated SiC VJFET and JBS diode and (b), the circuit symbol for the integrated device that can be used as a common building block of many power electronic circuits.

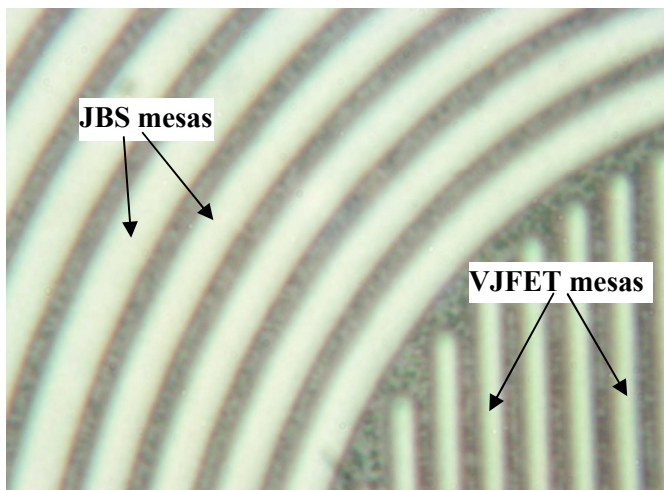


Fig. 2 An optical photo showing details of the SiC mesas for the VJFET and the JBS devices areas.

removing the N+ top ohmic contact epi. The rest of modifications only involves changes in the mask layout design.

The VJFET is designed to be normally-off and its channels need to be somewhat narrow. On the other hand, the JBS diode needs to have significantly wider channels to ensure good current capability. With the help of numerical simulations, the actual metallurgical channel openings of the JFET and JBS regions have been designed to be $0.4\mu\text{m}\sim 1.0\mu\text{m}$ and $2.5\sim 3.5\mu\text{m}$, respectively. Some variations have been included for each device for comparison. While the channel openings can be quite narrow, due to the sidewall P+ implantation, the mesa width is significantly wider. This makes the mesa aspect ratio less challenging for the anisotropic etching process. The channel lengths of the JFET and JBS structures are $2.5\mu\text{m}$ and $1.8\sim 2.0\mu\text{m}$, respectively.

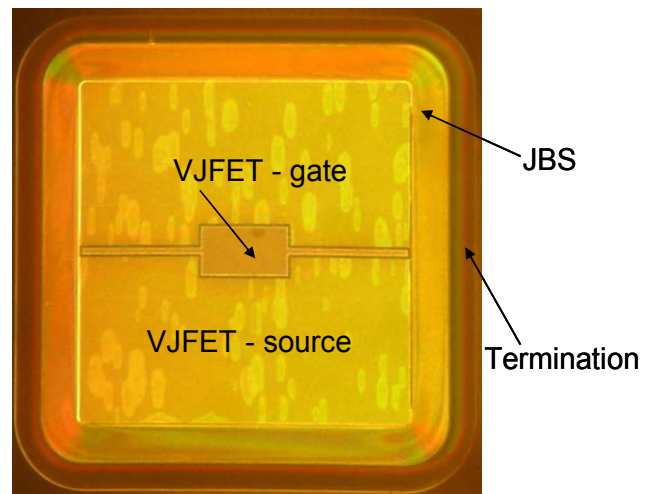


Fig. 3 An optical photo of the finished device.

The integrated VJFET-JBS device has been fabricated on 2" 4H-SiC wafer. Fig. 2 shows details of the SiC mesas in the VJFET and the JBS device regions during fabrication process. It is visible that the VJFET mesas are significantly narrower than those for the JBS.

A photo of the final finished device is shown in Fig. 3. The total device size is approximately $3\text{mm}\times 3\text{mm}$. As can be seen from the figure, the VJFET device is placed in the center of the device with its gate terminal sitting in the middle. It is enclosed by the JBS region that is made up of square-shaped mesa rings. The outer-most part of the device is the junction extension termination that gives the device its voltage blocking capability. The area of the VJFET is designed to be significantly larger than the JBS due to the following expectations.

- The free-wheeling diode usually conducts less RMS current than the main switch.

- When used in the “synchronous rectification” mode, the reverse conduction VJFET will help conducting the current and reducing the forward voltage drop of the diode.

The photo shows that the size of the VJFET/JBS integrated device is only slightly bigger than that of a simple VJFET, significantly saving total chip size.

III. DEVICE CHARACTERIZATION

The fabricated VJFET/JBS device has been characterized on the wafer level. The measured I_{DS} - V_{DS} curves have been plotted in Fig. 4 for both the forward and reverse current direction for gate voltages ranging from -6V to +4V. The forward output characteristics are typical of a JFET with a threshold voltage (V_{th}) of close to zero.

The *unique characteristics* of such an integrated device are reflected in its reverse I-V curves. The reverse I-V curves include both JFET and JBS current components. With a JFET channel threshold voltage close to zero, with $V_{GS}=-6V$ and $V_{DS}>-3V$, the JFET channel is completely off. The device reverse current shown in the lowest-current curve in the figure only comes from the JBS diode, which reveals a Schottky barrier of approximately 1eV. For V_{GS} less than -2V, the device reverse I-V curves overlap each other. As V_{GS} increases to above -1V, the JFET channel starts to turn on when V_{DS} decreases below -1V. The JFET channel current starts to dominate against the JBS component when V_{GS} rises above 2V. It should be noted that V_{GS} can rise above 3V due to some on-chip parasitic gate resistances.

This unique I-V curve is advantageous when the JFET is utilized in the reverse conduction mode to help the JBS. For the I-V curves shown, at 2A reverse current, the conduction voltage drop of the JBS can be reduced from 3V to 1.4V when the reverse-conduction of the JFET is used. *This means that a*

>50% reduction in the diode conduction loss can be achieved in the circuit.

For comparison and reference, the I-V curves of a smaller test structure with only the VJFET (0.078mm^2) fabricated on the same wafer has also been characterized and plotted in Fig. 5. Apart from a somewhat different JFET channel threshold voltage (around -2V), the biggest difference between this set of I-V curves and that shown in Fig. 4 is in their reverse characteristics. Without the JBS, the JFET channel is kept off more and more as its V_{GS} decreases and the reverse I-V curves are clearly separated from each other.

Another piece of useful information that can be extracted from Fig. 5 is the specific on-resistance of the VJFET device. With a device size of 0.078mm^2 , the VJFET specific on-resistance is found to be $3.7\text{m}\Omega\text{cm}^2$. This is considered to be quite reasonable for devices on this type of structures. The parasitic resistance introduced by the probe station setup has been excluded.

With an $11\mu\text{m}$, $9\times 10^{15}\text{cm}^{-3}$ N⁻ drift region epi, forward blocking voltage of the devices on this wafer is designed to be $\sim 1.2\text{kV}$. The forward blocking I-V curves of a test P-i-N structure fabricated on the wafer is plotted in Fig. 6. While the device is a little leaky, it is able to block close to 1kV. This validates a reasonable termination structure which has been kept the same for all devices on the wafer, including the integrated VJFET/JBS, VJFET, P-i-N diodes and other testing structures.

However, forward blocking capabilities of the actual fabricated VJFET/JBS structures and VJFET devices are found to be low. Possible reasons may be related to the deep trench etching. The exact reasons for low blocking voltages are still being investigated and new fabrications based on improved wafer structures are on-going to identify and possibly address this problem. Results will be reported once

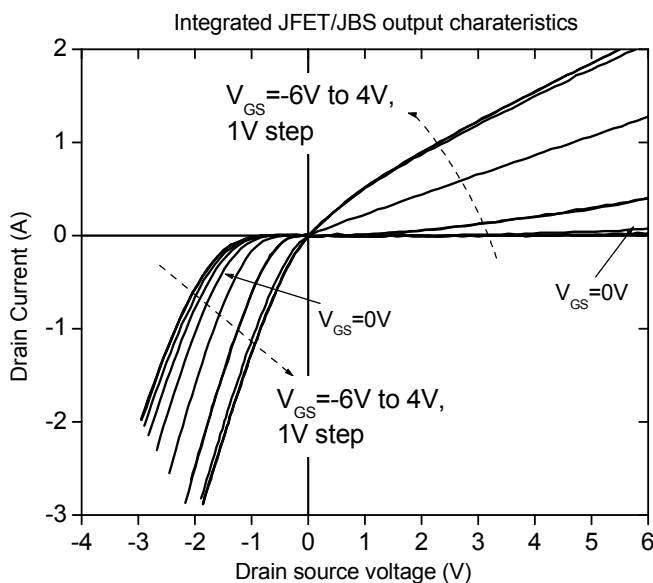


Fig. 4 Output characteristics of an integrated SiC JFET/JBS for both forward and reverse conduction.

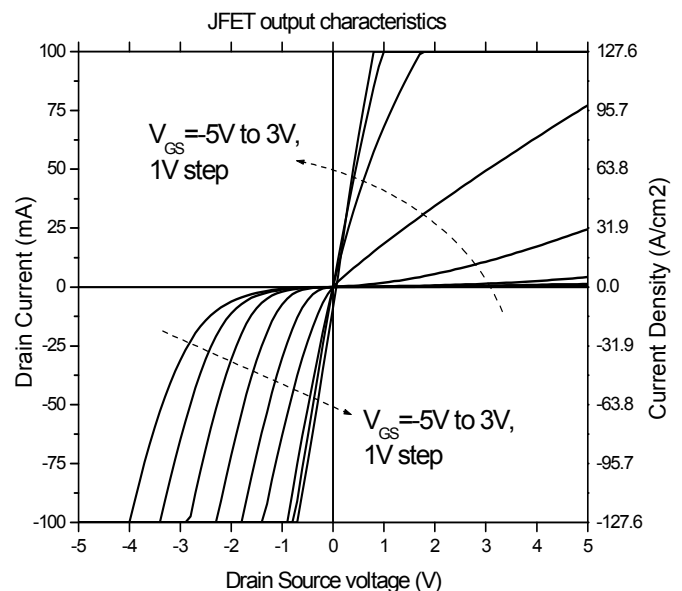


Fig. 5 Output characteristics of a test SiC JFET for both forward and reverse conduction.

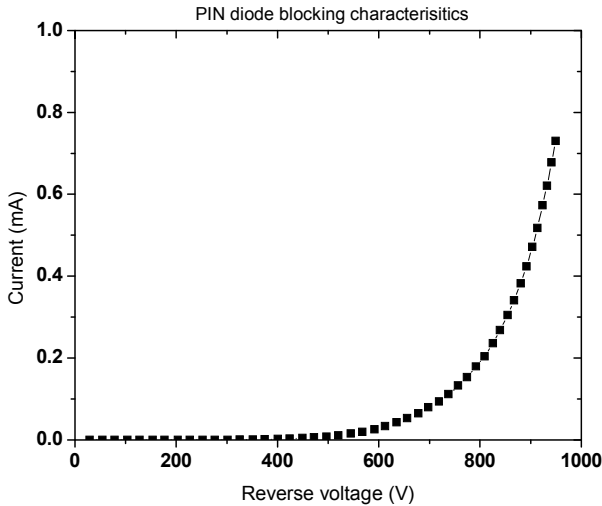


Fig. 6 Blocking I-V curve of a P-i-N test pattern fabricated on the wafer.

available.

IV. SUMMARY AND CONCLUSION

This paper proposes the concept and a detailed processing scheme of a vertical SiC JFET with an integrated JBS diode. The idea takes advantage of the similarity between the fabrication processes of the two devices and combines them monolithically. The integrated VJFET/JBS device only requires one extra major process step as compared to a simple VJFET.

The proposed idea has been successfully fabricated on 4H-SiC and the resultant devices characterized for both forward and reverse current conduction. It has been confirmed that the device can operate in the same way as two discrete chips connected in anti-parallel. In addition, the VJFET in the proposed device can be used in a “synchronous rectification”

mode that uses a reverse conducting VJFET to help the JBS in conducting reverse current. With this scheme, the reverse conduction voltage drop can be reduced by more than 50%. This can help reducing the area needed for the JBS device and hence also the total chip. It should be noted that such an advantage is not available in the SiC BJT/JBS integration scheme previously reported.

The proposed idea can be used as a fundamental building block for many power electronic applications. The integrated approach can reduce component count, improve reliability and reduce cost.

REFERENCES

- [1] Yan Gao, A. Q. Huang, A. K. Agarwal, and Q. Zhang, “Integration of 1200V SiC BJT With SiC Diode”, Proceedings of 20th International Symposium on Power Semiconductor Devices and IC’s (ISPSD), 2008, pp. 233 - 236
- [2] J. H. Zhao, K. Tone, X. Li, P. Alexandrov, L. Fursin and M. Weiner, “3.6 mΩcm², 1726V 4H-SiC normally-off trench-and-implanted vertical JFETs”, Proceedings of 15th International Symposium on Power Semiconductor Devices and IC’s (ISPSD), 2003, pp. 50 - 53
- [3] Y. Li, P. Alexandrov and J. H. Zhao, “1.88-mΩcm², 1650-V Normally on 4H-SiC TI-VJFET”, IEEE Transactions on Electron Devices, Vol. 55, Issue 8, Aug. 2008, pp. 1880 – 1886
- [4] J-S. Lai, H. Yu, J. Zhang, Y. Li, K. Sheng, J. H. Zhao, and A. Hefner and F. Goodman, “Characterization of Normally-off SiC Vertical JFET Devices and Inverter Circuits,” Proceedings of IEEE IAS Annual Meeting, Oct. 2005, pp. 404-409.