Design of a Robust Non-uniform Guard Ring Edge Termination for Near-theoretical 5.9-kV 4H-SiC JBS Diodes

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Abstract

This letter reports the design and fabrication of a robust, processing tolerant non-uniform guard ring edge termination for high power SiC devices. A 4H-SiC Junction-barrier-Schottky diode based on a 45.4 μm, 1.4×10^{15} cm^{-3} n- epilayer and with the guard ring design blocks 5960V, which is 95% of the theoretical breakdown voltage This indicates that the non-uniform guard ring edge termination is an efficient and robust design, with its simplicity and processing tolerance. The diode conducts 87 A/cm^2 at 2.5 V, at a specific on resistance of 24 $m\Omega cm^2$, which is very close to the theoretical value of 23.3 $m\Omega cm^2$, taking the current spread effect into account..

Index terms

Guard ring edge termination, Silicon carbide, Junction-Barrier-Schottky (JBS) diode

I. INTRODUCTION

4H-silicon carbide is commonly considered as a promising material for high power and high frequency electronics because of its wider bandgap, three-times higher thermal conductivity and an order of magnitude higher critical electric field [1] compared to silicon. 4H-SiC power devices can achieve higher breakdown voltages using thinner and heavier doped drift layers of substantially lower resistivity compared to silicon and work at higher junction temperatures and higher levels of ionizing radiation. Junction edge termination is a crucial design issue for any high-voltage device. Optimum edge termination provides the maximum device breakdown voltage for a drift layer of given thickness and doping. Many special designs of edge termination have been discussed and reported in the literature including planar junction [2], field plate [3-5], guard rings [6-8], junction termination extension (JTE)[9-11], and highly resistive implanted surface region [12-13] methods.

Edge termination with multiple floating guard rings is an attractive approach due to its technological simplicity, and has been utilized in SiC power devices with breakdown voltage lower than 3 kV [14]. However, when the blocking voltage is higher, the number of rings increases, indicating more challenging processing requirements including fine lithography and implantation. In this work, we present the design and fabrication of a 5960 V JBS diode with 63 floating guard-rings with non-uniform spacing serving as device edge termination. The blocking voltage reaches 95% of the theoretical value of 6.3 kV, indicating that the non-uniform guard ring edge termination is an efficient and robust design with its simplicity and processing tolerance. The JBS diode

conducts forward current at a density of 87 A/cm^2 at 2.5 V. The differential specific on-resistance R_{SP_ON} is evaluated and analyzed.

II. DESIGN AND FABRICATION

Schematic cross-sectional view of the device is shown in Fig. 1. The 4H-SiC wafer used was manufactured by Cree, Inc., and included a 45.4 μm n-type drift epilayer with a doping of 1.4×10^{15} cm^{-3}. The p+ implanted floating guard rings at the periphery of the JBS diode and the p+ regions within the active JBS diode area were formed by multi-energy simultaneous Aluminium ion implantation. The Al ion implantation energies and doses were 360 keV (2.4×10^{14} cm^{-2}), 200 keV (1.6×10^{14} cm^{-2}), 100 keV (8×10^{13} cm^{-2}) and 50 keV (4×10^{13} cm^{-2}), respectively. The resultant "box"-like profile of Al implants was 0.6 μm deep with a concentration of 1.2×10^{19} cm^{-3}. In the active area of the JBS diode, the p+ implanted stripes were 2 μm wide and the Schottky regions between them were 7 μm wide. Device edge termination included 63 p+ implanted guard rings of 2.5 μm width. The spacing between implanted guard rings increased from 0.8 μm at the innermost ring to 2.8 μm at the outmost ring, with increments of 0.1 um, and each spacing was repeated 3 times, as depicted in Fig. 1. Al implants were activated by annealing at 1550 ^{o}C for 30 min in ultra-high purity Ar ambient. Surface passivation consisted of a 3-hour thermal oxidation in wet oxygen at 1100 ^{o}C and, finally, a PECVD deposition of 200 nm SiO_2 and 300 nm Si_3N_4. Subsequently, the oxide was removed from the wafer backside, and a Ni layer was sputtered and annealed at 1100 ^{o}C for 5 min in Ar/H_2 gas mixture to form n-type cathode ohmic contact. The Schottky window was opened in the passivation layer by dry etching Si_3N_4 in inductively coupled plasma and wet etching SiO_2 with buffered oxide etchant. A Ti (80 nm)/TiW (250 nm) layer was

deposited in the window and annealed at 550 ^{o}C in Ar ambient for 20 min. This annealing improved the quality of Schottky interface between SiC and Ti. Finally, a thick Ti/Au overlay was deposited above the Schottky contact to further improve the forward current capability.

III. CHARACTERIZATION

The fabricated 4H-SiC JBS diodes were characterized at wafer level. JBS diodes combine the advantages of both PiN and Schottky diodes. They offer low leakage current in the off-state like the PiN diode and low forward voltage drop and fast switching characteristics like the Schottky diode [15]. High-voltage blocking test was performed on the JBS diode in standard 3M-Fluorinert dielectric liquid at room temperature. The reverse characteristics were tested up to 5960V with a leakage current of 0.93 mA, which corresponds to a current density of 800 mA/cm^2. Fig. 2 shows that the reverse leakage is 1.1 μA at 3000 V reverse bias. The theoretical breakdown voltage for ideal parallel-plane structure without edge field-crowding effects is 6.3 kV.

The optimum guard ring structure for the highest blocking voltage was identified through computer simulation with ISE-TCAD software. Two floating guard ring edge termination structures were considered and simulated. The first design approach was a traditional guard ring edge termination with 50 p+ implanted rings of 2.5 μm width and identical (uniform) spacing between them. Computer modeling shows that the blocking voltage reaches its maximum of 5.3 kV when the spacing is 1.5 μm and decreases if the spacing becomes wider or narrower. Fig. 3 (a) shows the surface electric field distribution through the guard rings under the applied reverse bias of 4.9 kV, for guard ring spacing of 1.5 μm. The highest electrical field of 3.3 MV/cm is at the innermost ring, where the

avalanche breakdown would occur when the applied voltage was higher than the blocking voltage. In our second design approach, the guard ring number and the ring width were kept the same. However, the spacing between adjacent rings was designed to increase from 1.0 μm at the innermost ring to 2.6 μm at the outmost ring with increments of 0.1 um. To achieve optimized blocking performance and tolerate possible line-width non-uniformity during the actual photolithography and ion implantation process, each guard ring spacing was repeated 3 times until the 50th ring. Fig. 3 (b) shows that under the same reverse bias of 4.9 kV, the electric field through the rings is more uniform than in the first design approach; and the highest electric field is as low as 2.58 MV/cm. It should be pointed out that the highest electric field does not occur at the outmost or the innermost rings, but at some middle rings. It makes the second design approach with non-uniform guard ring spacing more robust and better applicable for actual fabrication. Computer modeling of this design shows a blocking voltage of about 5900 V. In the actual diode fabrication, considering the photolithographic line-width non-uniformity across the wafer and other uncertainties introduced during the dry etching and implantation, we used 63 guard rings with the spacing increasing from 0.8 μm to 2.8 μm in the way described in the second design, making sure that the spacing from 1.0 μm to 2.6 μm will be fully covered. The experimental breakdown voltage of the fabricated JBS diode is 5960 V which is practically the same as the computer simulation result and is as high as 95% of the ideal parallel-plane breakdown voltage, indicating that an efficient edge termination is achieved. It should be pointed out that the whole processing of the guard ring termination involved only one photolithography and one implantation, indicating the simplicity of the process compared to other edge terminations for this blocking voltage range.

Under forward bias, the device current was characterized at room temperature and the results are shown in Fig. 4. The circular JBS diode with anode diameter ϕ=400 μm conducts anode current at a density of 86A/cm^2 at forward voltage drop of V_F = 2.5 V. Extrapolation of the linear J-V plot shows a turn-on voltage of 0.85 V and the differential specific on-resistance R_{SP_ON} = 19.2 mΩcm^2. As a comparison, the forward characteristics of a SBD of the same size fabricated on the wafer are also presented in the figure. The SBD has a R_{SP_ON} of 18.2 mΩcm^2 and the same turn-on voltage as the JBS diode. For high-voltage Schottky and JBS diodes, the series resistance of the thick drift layer is the dominant contributor to the specific on-resistance, which can be expressed as:

$$R_{SP_ON} = D / q\mu N_D$$

where D is the drift layer thickness, N_D the doping concentration, and μ the carrier mobility, which is 935 cm^2/Vs, according to our computer modeling. For the designed structure the theoretical value of R_{SP_ON} is 22 mΩcm^2. It should be pointed out that the experimental specific on-resistance evaluated using anode current density is less than the theoretical R_{SP_ON}. This is because in reality the electrical current is not confined within cylindrical region of 400μm diameter below Schottky contact, but spreads laterally outside that region through the thick drift layer [16]. Although the current density decreases rapidly away from the 400 μm cylindrical region, the current spreading is not negligible. With the current spreading effect taken into account, a computer simulation was performed to determine the specific on-resistance of the JBS diode. First, a Schottky barrier height of 1.14 eV and an ideality factor of 1.03 were determined from the experimental forward I-V curve of the Ti/4H-SiC Schottky diode, which was fabricated simultaneously with the JBS diode on the same wafer. The electron mobility at room

temperature was determined from the best fit to the forward I-V characteristics of the Schottky diode over the forward bias range from 0 to 2.5 V. Fig. 4 shows excellent agreement between computer modeling results and experimental data, which yields an electron mobility of 935 cm^2/Vs. The computer modeling of the forward I-V curve of the JBS diode was performed using the experimentally determined electron mobility of 935 cm^2/Vs and Schottky barrier height of 1.14 eV. The simulation results fit very well with the experimental data also shown in Fig. 4. Computer simulation with ISE-TCAD software can provide current density distribution throughout any cross-section of the device. For any small area on the bottom of the drift layer, which is a certain distance away from the axis of symmetry of the device, we can define the specific on-resistance using current density through that small area. The inset to Fig.4 shows that the so-defined R_{SP_ON} stays at about 24 $m\Omega cm^2$ within a distance of 150μm from the axis of symmetry of the device and increases rapidly, once outside 200μm from the device center. Therefore, if all the current fell into the active area of 400 μm diameter, we would get R_{SP_ON} = 24 $m\Omega cm^2$, which indicates that a nearly ideal forward I-V characteristic is achieved.

IV. CONCLUSION

In conclusion, the first 4H-SiC JBS diode designed with a robust edge termination, using 63 implanted guard rings of non-uniform spacing, ranging from 0.8 μm to 2.8 μm, has been fabricated successfully to block 5,960 V, which is nearly 100% of the design target and 95% of the theoretical parallel-plane breakdown voltage of the structure. The non-uniform guard ring edge termination is an efficient robust design with its simplicity and processing tolerance. The experimental specific on-resistance is found to be 19.2

mΩ.cm^2 when the current density is measured at the anode side. Computer simulation reveals that the JBS diode has a R_{SP_ON} of 24 mΩ.cm^2 when the current spreading effect in the drift layer is taken into account. This experimental R_{SP_ON} has reached the theoretical limit of the structure, considering possible drift variations in drift layer doping..

V. REFERENCES

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Figure Captions:

Fig. 1. Schematic cross-sectional view of the 4H-SiC JBS active area and floating guard ring edge termination.

Fig. 2. Comparison of experimental I-V characteristics of the PIN, SBD and JBS diodes.

Fig. 3. Computer simulation of electric field intensity for 2 different guard ring edge termination designs: a) Electric field distribution in 50 guard rings with uniform spacing under an applied reverse bias of 4.9 kV. The peak field of 3.3 MV/cm occurs at the innermost ring; b) Electric field distribution for the guard rings with non-uniform spacing from 1 um to 2.6 um. The peak field is 2.58 MV/cm.

Fig. 4. Experimental and computer modeling results of the forward I-V characteristics of the JBS and Schottky diodes, illustrating the Schottky barrier height of 1.14 eV and electron mobility of 935 cm^2/VS. The inset shows the differential specific on-resistance (R_{SP_ON}) of JBS diodes at the cathode side versus distance from the center of the diode.

Fig. 1

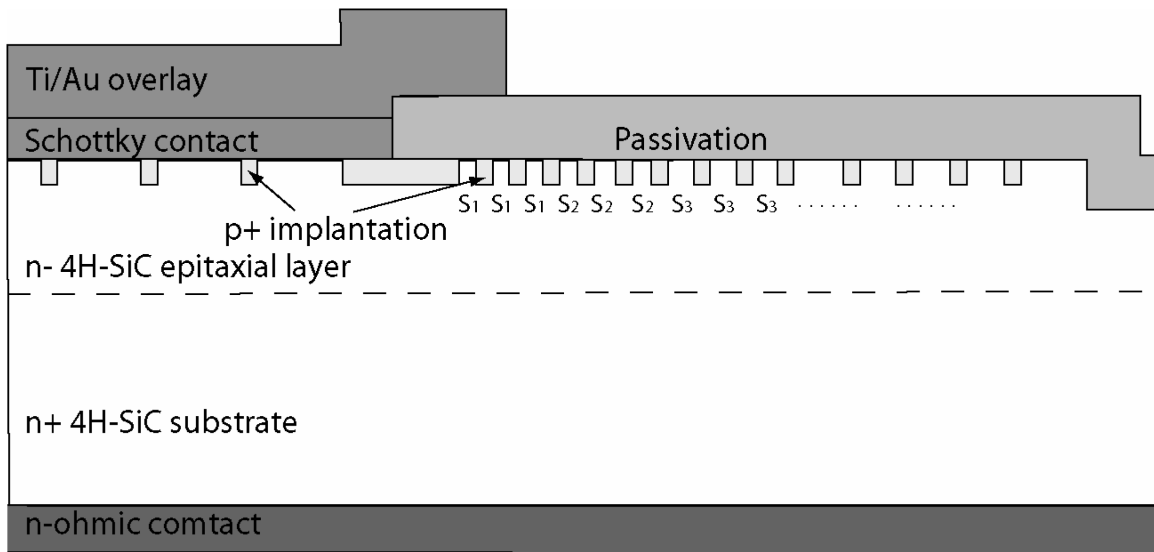

Fig. 2

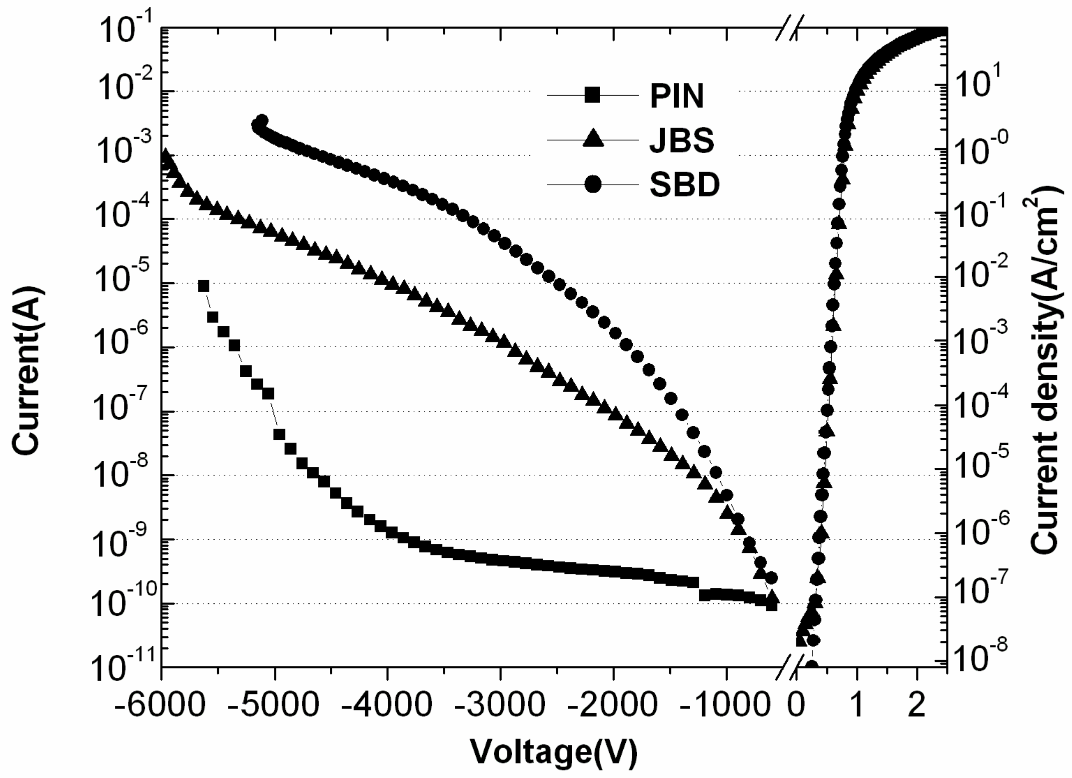

Fig. 3

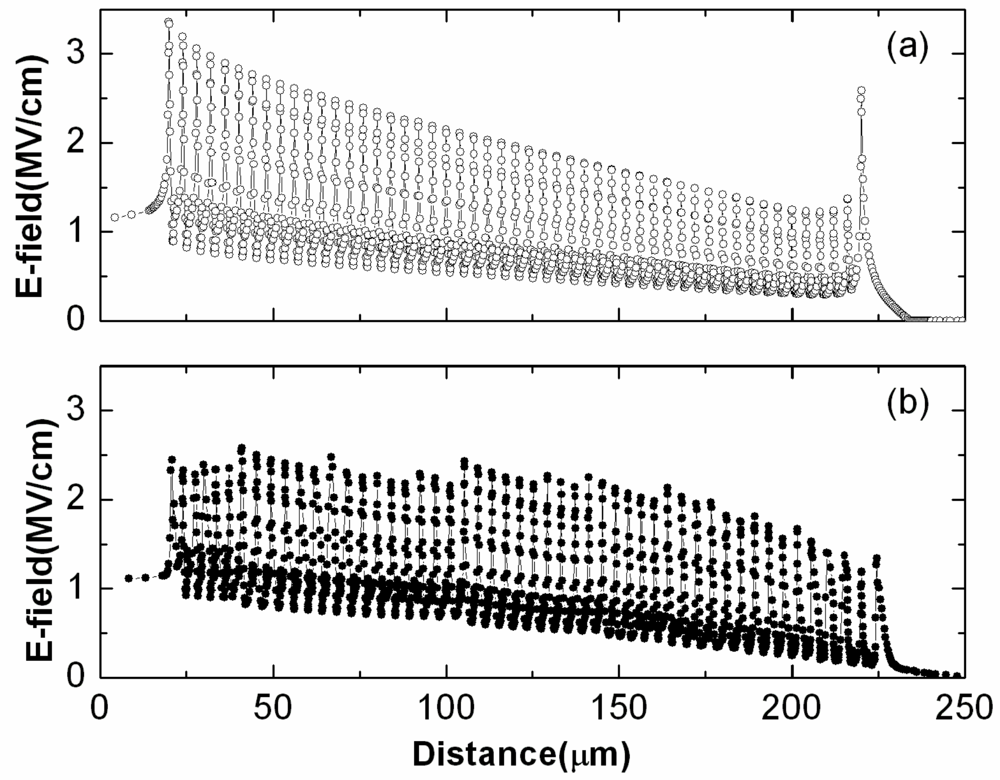

Fig. 4